Impact of Polysilicon Emitter Interfacial Layer Engineering on the $1/f$ Noise of Bipolar Transistors

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***Abstract*—To optimize the electrical characteristics of polysilicon emitter bipolar transistors, the poly emitter interface needs careful engineering. In this paper, bipolar transistors of a 0.5 μm BiCMOS process have been fabricated with intentionally grown oxides in an LPCVD cluster for precise control over the interfacial oxide thickness and uniformity. The trade off between current gain enhancement and increased $1/f$ noise will be discussed for various interfacial oxide thicknesses and emitter annealing conditions. It will be demonstrated that for sufficiently large base currents, both for large ($20\,\mu$m $\times$ $20\,\mu$m) and small ($0.5\,\mu$m $\times$ $5\,\mu$m) emitter areas the interfacial oxide dominates the $1/f$ noise spectrum of the base current. Hence, the polysilicon emitter interface engineering will not only set the current gain at a predefined value, but at the same time the associated oxide-tunnelling noise is fixed, within the constraint that the emitter-base junction depth is constant. Finally, it will be shown that the current gain enhancement and increased $1/f$ noise have compensating effects on the output noise of practical circuits.**

I. Introduction

TODAY'S high performance bipolar technologies rely upon precise control of the interfacial oxide between the polysilicon emitter contact and the underlying substrate. Using a conventional horizontal LPCVD deposition tube, the pre-cleaning and deposition processes must be carefully engineered in order to give reproducible electrical characteristics. Since the pre-cleaning and deposition processes are not *in situ* some re-oxidation of the silicon surface can occur during the wafer loading operation due to back streaming of oxygen. In order to ensure good control of the interfacial layer the furnace temperature and flow rates must be carefully optimized [1]. The advent of LPCVD cluster tool technology allows precise control of the interfacial oxide layer through the use of *in situ* HF vapor cleaning and subsequent re-oxidation prior to polysilicon deposition [2]. This gives a more flexible process for optimization of the transistor parameters toward high emitter efficiency and low emitter resistance. This optimization is essential for realizing transistors with good mixed analog and digital performance.

For high frequency analog applications the transistor $1/f$ noise is also an important parameter since it can degrade the spectral purity of the circuit. While the impact of the interfacial oxide thickness and the amount of oxide break-up on the dc characteristics is well established, the impact on the $1/f$ noise behavior is not well characterized and the noise mechanisms are not fully understood. First results point at an increased $1/f$ noise level when the interfacial oxide thickness increases [3]–[10]. There is also some evidence that the $1/f$ noise spectral density in the low and in the high current region have a different physical origin [8] and [10].

In this paper, the impact of the interfacial oxide thickness on the $1/f$ noise will be investigated using samples processed in an LPCVD cluster tool. The $1/f$ noise in the low and high base current I_B region will be investigated as a function of the interfacial oxide thickness and the emitter anneal, in case of RTA or furnace anneal. For reasons of comparison, BJT's with the polysilicon emitter deposited in a conventional horizontal tube will also be included. For the latter samples, it will be shown that the RTA temperature allows precise control over the current gain, and the corresponding impact of different RTA temperature on the $1/f$ noise will be discussed. It will be demonstrated that irrespective of the deposition technique or annealing conditions, for transistors with comparable emitter junction depths, a one to one correlation exists between the base current suppression and increased $1/f$ noise.

The paper starts with a description of the processing of the bipolar transistors with special emphasis on the poly emitter processing (Section II). The poly emitter interface and the emitter/base impurity profiles will be characterized in Section III. The impact on the current gain and emitter resistance will be summarized in Section IV. In Section V, the $1/f$ noise characteristics will be discussed in detail for different process conditions, and the consequences of the interface engineering for low noise amplifier design will be commented.

II. Device Fabrication

As the basis for our study we have used the bipolar transistors of a 0.5 μm high performance (15 GHz) mixed analog/digital, single poly BiCMOS process [2]. The transistors have a quasiself-aligned emitter/base architecture in which the poly emitter contact is defined using an emitter window cut in a thin base oxide layer and the PMOS LDD and HDD regions are self-aligned to the edge of the polysilicon emitter contact using the CMOS spacer process. The emitter window is opened in the base oxide by dry etching, followed by NF_3 post-etch cleaning to remove the etch residues [11]. A Ti-

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TABLE I
DETAILS OF THE VARIOUS POLYSILICON INTERFACE ENGINEERING APPROACHES USED IN THIS WORK AND INTEGRATED OXYGEN DOSE, MEASURED BY SIMS

Deposition Equipment	Pre-clean	D_{ox} RTA 1100°C ($x10^{15}$ cm^{-2})	D_{ox} Furnace 900°C ($x10^{15}$ cm^{-2})	Oxidation Time
Horizontal	HF-dip	1.9		--
Furnace	HF-dip		1.9	--
Cluster	HF-dip	1.0		no reoxid.
	HF-vapour	0.9		no reoxid.
Cluster	HF-vapour	1.6		3 min.
	HF-vapour		1.6	3 min.
	HF-vapour	2.2		30 min.
	HF-vapour		2.1	30 min.
	HF-vapour	2.6		180 min.
	HF-vapour		2.7	180 min.

silicide is used to reduce the external base resistance and the emitter resistance.

Wafers were processed at emitter polysilicon deposition either in an ASM Advance/600 LPCVD cluster tool or in a conventional horizontal LPCVD system. Wafers processed in the cluster system were first given an *in situ* HF vapor clean and were then transferred under 1 Torr nitrogen to a vertical LPCVD poly tube. Thermal re-oxidation of the wafers was then performed for several oxidation times prior to 350 nm poly deposition at 620 °C, as summarized in Table I. The RTA emitter drive was carried out at 1100 °C for 10 s to break-up the interfacial layer, or at 900 °C for 20 min. in a furnace tube to leave it continuous.

Wafers processed in the conventional LPCVD tube were first given an 0.5% 120 s aqueous HF-dip before loading into the poly deposition system at 500 °C. The furnace was then pumped down and ramped to the deposition temperature of 620 °C. This procedure is necessary in order to avoid excessive or uncontrolled regrowth of oxide. For these wafers the RTA emitter anneal was carried out at either 1075, 1100, or 1125 °C for 10 s. In addition, some wafers were also given an RTA pre-anneal at 1025 °C for 10 s, before As implantation, since the interfacial oxide breaks up more easily in absence of the high arsenic concentration.

III. DOPING PROFILE AND INTERFACIAL LAYER EVALUATION

In order to give a quantitative measure of the thickness of the interfacial oxide layer, the oxygen profile at the poly-mono interface has been measured using SIMS [2]. Table I summarizes the oxygen dose D_{ox} measured for the different splits. From the first two entries in this table, we observe that the *in situ* HF-vapor clean is as efficient in removing the native oxide from the wafers as the HF-dip in aqueous HF solution.

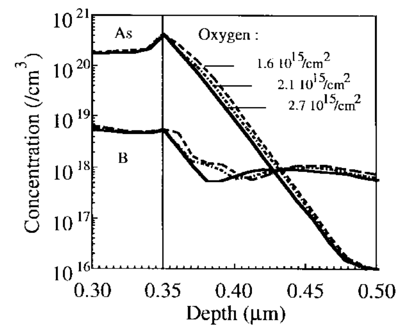

Fig. 1. Arsenic and boron profiles in the vicinity of the polysilicon emitter interface, for different oxygen doses. Furnace anneal.

When using a conventional horizontal polysilicon furnace, the amount of oxygen at the interface can not be so readily controlled. With our present procedure, we obtained an integrated oxygen dose of 1.9×10^{15}/cm^2. Using low temperature thermal reoxidation for 3, 30, and 180 min, the integrated oxygen dose can be increased from the 1.0×10^{15}/cm^2 level obtained without any reoxidation (polysilicon deposition immediately after the HF-vapor clean) to respectively 1.6×10^{15}, 2.2×10^{15}, and 2.6×10^{15}/cm^2. Remark that the dose that was obtained using the horizontal poly furnace is within this range.

In Fig. 1, the arsenic and boron emitter/base SIMS profiles in the vicinity of the interface are shown for different oxygen doses, for samples with furnace anneal (FA). The higher the oxygen dose, the more the emitter outdiffusion from the poly emitter to the monocrystalline substrate is suppressed, although the total difference in outdiffusion is smaller than 10 nm. The boron profiles are also slightly affected because of the emitter push effect, as is evidenced by the shift in the location of the notch in the base profile. The relatively high concentration of boron in the emitter poly is a feature of the CMOS compatible emitter-base structure and is due to the PMOS HDD implant. For the RTA annealed samples (Fig. 2), a similar suppression of the emitter outdiffusion with increasing oxygen dose is observed. The exception to this is the sample with the lowest oxygen dose where epitaxial realignment has affected the impurity profiles. This was confirmed by Rutherford Back Scattering channeling spectra which indicated that the polysilicon layer had epitaxially re-aligned over approximately one fifth of its thickness.

IV. DC CHARACTERISTICS

The quasi-self aligned emitter base structure provides an excellent vehicle for analyzing base current suppression and noise behavior due to the ideal behavior of the dc characteristics. From the characteristics reported earlier [2], we deduce that the current gain is constant over more than five decades of the collector current. The base current suppression with increasing oxygen dose is clearly observed while from the collector characteristics we conclude that I_C is only weakly depending on the oxygen dose. This is in agreement with the SIMS doping profiles which showed minor differences in emitter outdiffusion. Because the collector current is only a weak and indirect function of the oxygen dose, effects on the collector current will be further neglected, especially in view

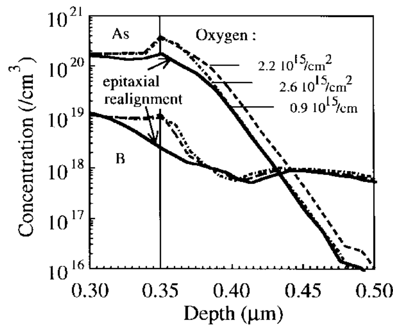

Fig. 2. Arsenic and boron profiles in the vicinity of the polysilicon emitter interface, for different oxygen doses. RTA anneal.

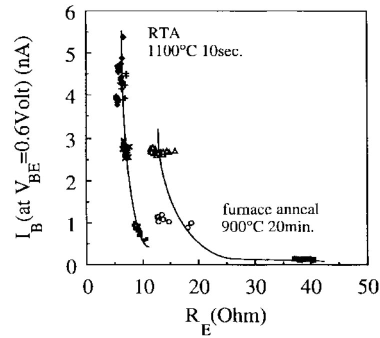

Fig. 4. Base current versus emitter resistance for different oxygen doses. RTA and furnace anneal. $A_E = 1\,\mu\text{m} \times 20\,\mu\text{m}$.

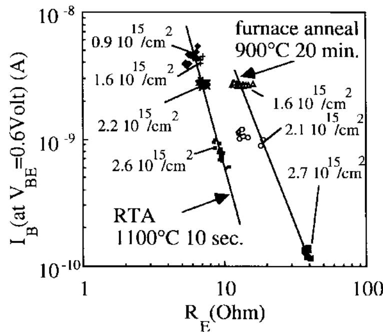

Fig. 3. Base current versus emitter resistance for different oxygen doses. RTA and furnace anneal. $A_E = 1\,\mu\text{m} \times 20\,\mu\text{m}$.

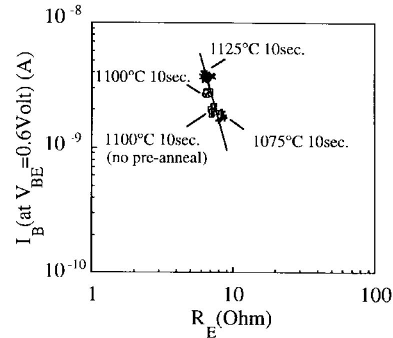

Fig. 5. Base current versus emitter resistance for different RTA temperatures. $A_E = 1\,\mu\text{m} \times 20\,\mu\text{m}$.

of the strong dependence of the base current on the interfacial oxide thickness and anneal conditions.

In Fig. 3, the base current at a V_{BE} bias of 0.6 V is plotted versus the emitter resistance, for transistors with different oxygen doses at the interface. Two separate sets of data are found. For the RTA annealed transistors, the strong suppression of the base current for increasing oxygen doses is clearly observed. This strong suppression is traded off against an increase of the emitter resistance R_E. For the furnace annealed transistors, a similar base current versus emitter resistance trade off is obtained, but the whole curve is shifted toward higher values of the emitter resistance, because the interfacial layer remained intact during the furnace anneal, while it is broken up for the RTA.

The data of Fig. 3 are shown on a double logarithmic scale, in order to demonstrate that the base current versus emitter resistance trade off exists over the full range of oxygen doses that was used. However, from a practical point of view, the data replotted on a linear scale (Fig. 4) show that there exists a region for the RTA annealed transistors where the base current can be suppressed with minimal impact on the emitter resistance, because the I_B–R_E curve is very steep.

When transistors are fabricated using a conventional horizontal poly furnace, the amount of oxygen at the interface cannot be so readily controlled. However, it is still possible to engineer the I_B–R_E operating point by changing the temperature of the RTA or by including a pre-implant poly anneal, as shown by Fig. 5. The range over which the base current can be engineered for a given oxygen dose at the interface is limited, since lowering the RTA temperature below the threshold temperature for oxide break-up will result in a deviation from the RTA anneal curve toward the higher values exhibited for the FA devices.

Combining the I_B–R_E data for all devices which received an RTA anneal, we conclude that despite the differences in the poly deposition conditions in the two systems they share a common I_B–R_E relationship. In other words for both depositions, engineering of the base current suppression for minimum impact on the emitter resistance is possible but in the case of the cluster an additional degree of freedom is afforded by the *in situ* oxidation. In the conventional deposition case the RTA temperature can be optimized toward maximum base current suppression but the range may be limited by threshold temperature for oxide break-up.

Having established the polysilicon interface engineering for the dc characteristics, it will be investigated in the next section whether this has an impact on the $1/f$ noise behavior of the transistors.

V. $1/f$ Noise Characterization

A. The Low Frequency Noise Spectral Density

In this work low frequency noise measurements have been performed in the common emitter configuration using source resistance R_S corresponding to both high impedance (HI) and low impedance (LI) modes of operation (i.e., with source resistances R_S which are either much larger (HI) or lower (LI) than the input impedance of the transistor). The collector voltage in all cases is fixed at $V_{CE} = 3$ V. Two device

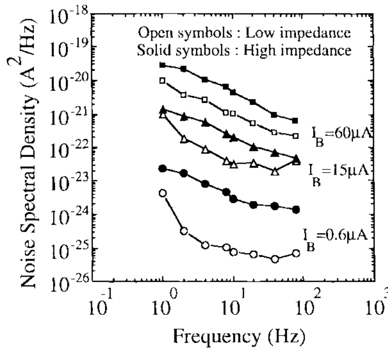

Fig. 6. HI (solid symbols) and LI (open symbols) spectra obtained for a $20\,\mu$m × $20\,\mu$m transistor. Standard furnace deposition and 10 s 1075 °C RTA has been used.

geometries have been studied in detail having emitter areas A_E $(= W_E \times L_E)$ of $20\,\mu\text{m} \times 20\,\mu$m and $0.5\,\mu\text{m} \times 5\,\mu$m. In Fig. 6 typical HI and LI input-referred spectra are shown for a device with a 20 μm emitter width processed in the conventional deposition furnace. The spectra exhibit a $1/f^\gamma$ type behavior with γ close to unity over the range of base currents and frequencies studied (between 1 Hz and 1 kHz). Similar results have been obtained for the devices processed in the LPCVD cluster. In general, over the range of devices considered in the present work, we have found that the frequency exponent γ varies between a maximum value of 1.1 at high base currents to a minimum value of 0.85 for the lowest base currents. Such a variation with current level has also been observed in Si MOSFET's [12]. In contradiction to other reports [3] and [9], so far, little Lorentzian-like noise components have been observed in the spectra.

Several noise sources can potentially contribute to the $1/f$ output noise spectral density [9], [13], [14]. To identify the dominant $1/f$ noise mechanisms, measurements at high and low source impedance R_S have been compared, as in Fig. 6. $R_S = 100\,\Omega$ for the low impedance measurements, while for the high impedance measurements, R_S is chosen as $R_S = (V_s - V_{BE})/I_B$ with V_S the supply voltage, which guarantees $R_S \gg r_\pi = V_T/I_B$. Hereby is V_T the thermal voltage and r_π is the base-emitter junction dynamic resistance. Comparing the common-emitter HI with the LI results, a clear reduction in the $1/f$ noise is observed, from which it is concluded according to [4] that the dominant noise current source for high impedance measurements is the base $1/f$ noise current amplified by β^2 to the output, with β the current amplification. Hence, the base current $1/f$ noise spectral density $S_{Ib}(f)$ can in good approximation be obtained from measurements with high source impedance of the output noise spectral spectrum $S_{Vo(f)}$ across the load resistance R_L by [8] and [14]

$$S_{Ib}(f) = \frac{S_{Vo}(f)}{R_L^2\,\beta^2}. \tag{1}$$

The $1/f$ base noise current spectral density for a polysilicon emitter BJT consists of several contributions, which can be represented as follows [6] and [9]

$$S_{Ib}(f) = S_{Ib,diff} + S_{Ib,rec} + S_{Ib,t} \tag{2}$$

whereby the first term corresponds to the diffusion noise (or mobility fluctuations component), which is proportional to the ideal part of the base current. The second term corresponds to the fluctuations in the nonideal part of the base current and is mainly dominated by recombination at the surface of the emitter/base depletion region [15]. This term is proportional to the square of the base/emitter recombination current component, having an emission coefficient $1 < m < 2$. The third term corresponds to fluctuations in the interfacial oxide tunnelling barrier, for which different expressions can be found in the literature [5]–[8]. However, in all cases it is found that the associated noise term varies with I_B^2. The latter component has been shown to be the dominant source of excess $1/f$ noise in polysilicon BJT's [5]–[8] and is strongly determined by the applied interface engineering, which will be demonstrated in the next section.

B. Influence of the Oxygen Dose at the Interface on the $1/f$ Noise

In order to evaluate the influence of the interfacial layer processing on the $1/f$ noise we now restrict our analysis to the noise spectral density at 10 Hz which is well into the $1/f$ noise region for the HI measurements. In Fig. 7, the base current noise spectral density is shown as a function of the dc base current, for transistors processed in the LPCVD cluster with different oxygen dose at the interface. The emitter area is $A_E = 20\,\mu\text{m} \times 20\,\mu$m. Two regimes in the base current dependence can be distinguished for the base current range investigated ($0.5\,\mu\text{A} < I_B < 50\,\mu\text{A}$), in agreement with recent reports [8] and [10]. In the high current region, a strong increase of the $1/f$ noise is observed with increasing oxygen dose at the interface. For the same oxygen dose, the noise is significantly higher in the case of furnace anneal (FA) compared to RTA. In this region, the noise spectral density is in good approximation proportional to I_B^2. We conclude from this that the dominant noise mechanism for both types of device can be identified as tunnelling barrier fluctuations. In the low current region, the curves converge and the impact of the process conditions diminishes. In this region the noise spectral density tends toward a proportionality of I_B or $I_B^{2/m}$ with m the emission coefficient of the emitter/base depletion region recombination current component. In this regime the noise cannot be measured accurately enough and over a sufficient I_B range to distinguish between the two dependencies. Measurements on small area devices from the same wafers are shown in Fig. 8. The same tendencies can be observed as for the large area devices. However, for a given base current the noise is much higher for small area devices. We have found this increase to be in agreement with the $1/A_E$ dependence which has been reported in other work [7]–[9].

The observed experimental trends can be summarized as follows:

$$S_{Ib}(f) = \frac{K_{ox} I_B^2}{f^\gamma} \tag{3a}$$

with K_{ox} a semi-empirical, dimensionless (if $\gamma = 1$) factor depending on the device area A_E and on the oxide thickness t_{ox} (in nm), or the integrated oxygen dose D_{ox} (/cm^2).

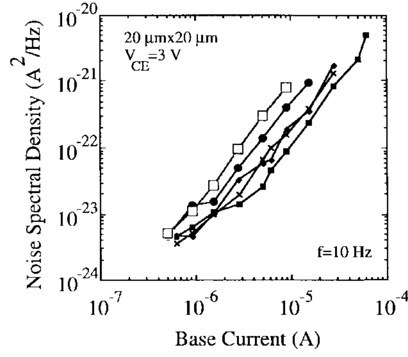

Fig. 7. Influence of the oxygen dose at the interface on the HI common emitter-base current noise spectral density, for $A_E = 20\,\mu\text{m} \times 20\,\mu\text{m}$ (deposition in an LPCVD cluster). The curves correspond, respectively, to: RTA $1.6 \times 10^{15}\,\text{cm}^{-2}$ (squares); FA $1.6 \times 10^{15}\,\text{cm}^{-2}$ (diamonds); RTA $2.2 \times 10^{15}\,\text{cm}^{-2}$ (x); FA $2.1 \times 10^{15}\,\text{cm}^{2}$ (full circles) and RTA $2.6 \times 10^{15}\,\text{cm}^{-2}$ (open squares).

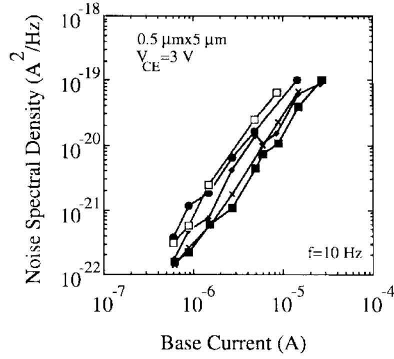

Fig. 8. Influence of the oxygen dose at the interface on the HI common emitter base current noise spectral density, for $A_E = 0.5\,\mu\text{m} \times 5\,\mu\text{m}$ (deposition in LPCVD cluster). The curves correspond, respectively, to: RTA $1.6 \times 10^{15}\,\text{cm}^{-}2$ (squares); FA $1.6 \times 10^{15}\,\text{cm}^{-2}$ (diamonds); RTA $2.2 \times 10^{15}\,\text{cm}^{-2}$ (x); FA $2.1 \times 10^{15}\,\text{cm}^{-2}$ (full circles) and RTA $2.6 \times 10^{15}\,\text{cm}^{-2}$ (open squares).

Equation (3a) is valid for sufficiently high I_B. However, when the transistor enters high injection, the empirical noise behavior starts to deviate. The analysis of the noise behavior there is out of the scope of the present work. For the RTA annealed $20\,\mu\text{m} \times 20\,\mu\text{m}$ transistors processed in the LPCVD cluster, K_{ox} equals

$$K_{ox} \approx 3.4 \times 10^{-13} \exp(2.02 \times 10^{15} D_{ox}) \tag{3b}$$

or, equivalently

$$K_{ox} \approx 4 \times 10^{-13} \exp(5.36 t_{ox}) \tag{3c}$$

with D_{ox} expressed in at/cm^2 and t_{ox} in nm. These values are derived from a least-squares fit to the experimental data points. For the FA annealed devices, similar values can be obtained, with a larger pre-factor value in (3b) and (3c). This pre-factor can be considered as a theoretical lower limit for the normalized noise performance of these transistors, corresponding to D_{ox} or $t_{ox} = 0$. In practice, this will result in strong epitaxial realignment, which is known to yield the lowest noise performance [7], but which also affects the impurity profiles.

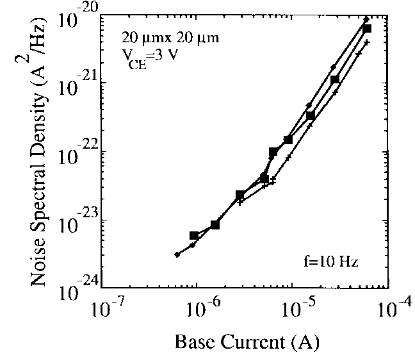

Fig. 9. Influence of the RTA temperature on the noise spectral density at $f = 10$ Hz, for $A_E = 20\,\mu\text{m} \times 20\,\mu\text{m}$. Oxygen dose at interface is $1.9 \times 10^{15}/\text{cm}^2$. The curves correspond to: 1100 °C (full squares); 1075 °C (diamonds); 1125 °C (+).

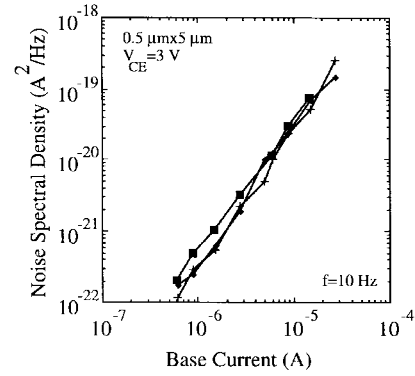

Fig. 10. Influence of the RTA temperature on the noise spectral density, for $A_E = 0.5\,\mu\text{m} \times 5.0\mu\text{m}$. Oxygen dose at interface is $1.9 \times 10^{15}/\text{cm}^2$. The curves correspond to: 1100 °C (full squares); 1075 °C (diamonds); 1125 °C (+).

C. Influence of the Oxide Break Up On the Noise Spectral Density

In the previous section, it has already been shown that a furnace anneal resulted in significantly higher noise spectral densities than an RTA, for transistors with the same oxygen dose at the interface. This thermal oxide break-up is now further explored by inspecting the noise spectral density for samples processed in the horizontal furnace with an oxygen dose of 1.9×10^{15}/cm^2 and different RTA conditions. In Fig. 9, for transistors with an emitter area of $20\,\mu\text{m} \times 20\,\mu\text{m}$, the noise spectral density is plotted as a function of the base current. Again, two regions in the bias dependence are observed. In the high current region, the noise spectral density is proportional to I_B^2 and the noise increases with decreasing RTA temperature. In the low current region, again a convergence of the curves is observed and the influence of the RTA temperature vanishes. For transistors with smaller area this trend is less clear in Fig. 10 due to the larger sample-to-sample noise variation.

It is clear from Figs. 7–10, that the amount of oxide break-up has a large impact on the $1/f$ noise, as is evidenced by the influence of the RTA temperature and the difference between RTA and furnace anneal. For the same oxygen dose at the interface the noise behavior can change dramatically depending on the annealing conditions. Hence, similar as for the

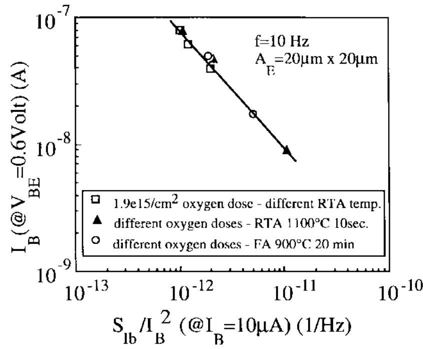

Fig. 11. Scatterplot of S_{Ib}/I_B^2 (@ $I_B = 10\,\mu$A and $f = 10$ Hz) versus I_B (@ $V_{BE} = 0.6$ V), for all splits studied.

base current versus emitter resistance trade off (Figs. 3–5), we conclude that engineering of the characteristics using a fixed oxygen dose and optimising RTA conditions, or optimising the oxygen dose for a constant RTA temperature lead to an equivalent influence on the $1/f$ noise spectral density. Hence, in addition to the base current suppression versus increased emitter resistance trade off, a trade off base current suppression versus increased $1/f$ noise spectral density exists (Fig. 11).

From Fig. 11, follows that there exists a one-to-one correlation between the base current suppression (represented by the base current at fixed $V_{BE} = 0.6$ V : $I_{B0.6}$) and the LF excess $1/f$ noise normalized by its base current dependency. For sufficiently high I_B, this relationship can be described by

$$f\frac{S_{Ib}(f)}{I_B^2} = -2.02 \times 10^{-12} + \frac{9.5 \times 10^{-19}}{I_{B0.6}} = -2.02 \times 10^{-12} + \frac{9.5 \times 10^{-19}\beta}{I_{C0.6}} \quad (4)$$

(for $I_B = 10$ μA, $f = 10$ Hz, and $\gamma \approx 1$), whereby the constant prefactor represents the part of K_{ox} that can not be controlled by the interface engineering approach. In other words, by the polysilicon interface engineering, not only the current amplification is selected, but at the same time the associated normalized oxide-tunnelling noise is fixed, within the constraints of a constant emitter-base junction depth, which is necessary to keep I_C approximately constant. Applying a larger junction depth has been shown to reduce the noise [7] and [9], because more holes can recombine in the crystalline emitter part. This would result in a parallel shift to the left of the straight line in Fig. 11. Reducing the junction depth gives rise to the opposite.

D. Impact of the Interfacial Layer Engineering on the $1/f$ Noise in Practical Circuits

The final question to be answered, is whether the improvement in dc characteristics is not jeopardised by the increase of the $1/f$ noise. In many practical circuits, the increased $1/f$ noise per unit of base current can be compensated by having a lower dc base current, due to the increased current gain. The simplified voltage amplifier of Fig. 12 illustrates this issue. The voltage amplification of the transistor is $A_V = -g_m \times R_L$. For identical voltage amplification, the g_m must remain constant, and since $g_m = I_C/V_T$ with V_T the thermal

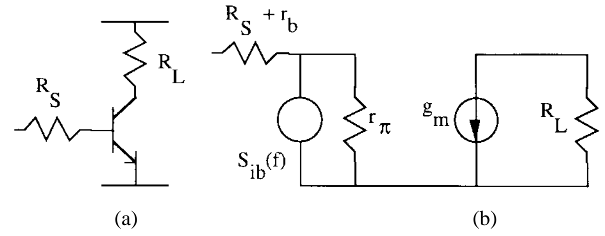

Fig. 12. Simplified voltage amplifier.

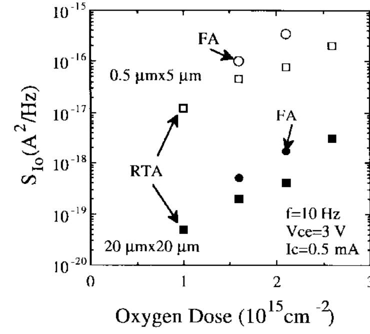

Fig. 13. Measured output current noise spectral density of amplifier circuit as a function of oxygen dose, at a fixed $I_C = 0.5$ mA. $f = 10$ Hz. High impedance signal source.

voltage, this implies a constant collector current. A transistor with high current gain results then in a lower I_B, and the lower I_B compensates for a higher $1/f$ noise per unit base current.

For a high impedance signal source, which is the worst case for transfer of base current noise toward the output, the output $1/f$ noise current spectral density $S_{Io}(f)$ equals

$$S_{Io}(f) = \beta^2 S_{Ib}(f) = \frac{I_C^2}{I_B^2} \times \frac{K_{ox} I_B^2}{f^\gamma} = \frac{I_C^2}{f^\gamma} \times K_{ox} \quad (5)$$

and hence the output spectrum is only linear proportional to K_{ox}. This is experimentally confirmed by the output noise spectral density for a voltage amplifier with $|A_V| = 20$ in Fig. 13, where indeed the proportionality with K_{ox} is observed, for different process conditions and emitter sizes.

For a low impedance signal source, on the other hand, we find:

$$S_{Io}(f) = S_{Ib}(f) \frac{(R_S + r_b)^2}{r_\pi^2} \beta^2 = \frac{K_{ox} I_B^2}{f^\gamma} (R_S + r_b)^2 g_m^2 = \frac{I_c^4}{f^\gamma V_T^2} (R_S + r_b)^2 \times \frac{K_{ox}}{\beta^2} \quad (6)$$

and hence the increase in K_{ox} is compensated by the increase in β^2. Also this is experimentally confirmed by the output noise spectral density of the amplifier circuit, as shown in Fig. 14, where indeed the LI noise for the $0.5\,\mu$m $\times$ $5\,\mu$m BJT's shows a slight reduction with t_{ox}, both for the RTA and FA devices, with the exception of the device with thickest interface oxide. The latter increase is not understood at the moment. For the large area devices, negligible excess $1/f$ noise is observed at 10 Hz (Fig. 6) in the LI configuration, so that this parameter is of no practical concern in that case.

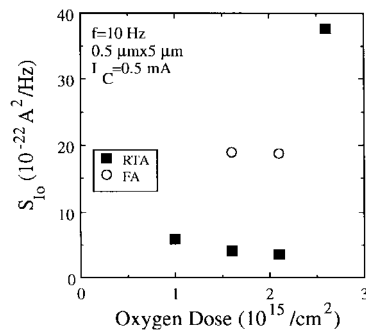

Fig. 14. Measured output current noise spectral density in the LI mode ($R_S = 100\,\Omega$), at $I_C = 0.5$ mA for the $0.5\,\mu$m $\times$ $5\,\mu$m polysilicon emitter BJT's.

VI. Conclusions

The polysilicon emitter interface can be engineered for base current suppression, but this is inevitably associated with an increase of the $1/f$ base noise current spectral density in the high current region. In this respect, engineering the amount of oxygen at the interface for a given emitter anneal, or engineering the emitter anneal for a fixed amount of oxygen at the interface are equivalent. Furthermore, this trade off can not be shifted by using more precise equipment to control the interface: the trade off is inherent to the tunnelling barrier. Derived from this trade off we can summarize that the $1/f$ base current noise spectral density will increase with increasing oxygen dose and with reduced oxide break-up. The above conclusions were valid in our experiments for large area (400 μm^2) and small area (2.5 μm^2) transistors.

In the low current region, the dependence of the $1/f$ base noise current spectral density on interfacial properties vanishes, while the current gain enhancement remains. As a consequence, the interface engineering of transistors for amplifier circuits results in increased or decreased $1/f$ noise depending on the dc bias and the impedance of the signal source: for the thick or unbroken interfacial oxides, the output noise will be higher at high dc bias currents and high source impedance, but it will be lower at low currents or at low source impedance.

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